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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,740	08/19/2003	Toshiyuki Kasai	116885	3821
25944	7590	11/03/2005	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			XIAO, KE	
			ART UNIT	PAPER NUMBER
			2675	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/642,740

Applicant(s)

KASAI, TOSHIYUKI

Examiner

Ke Xiao

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claims 1, 3, 13 and 29-30 are objected to because of the following informalities:

Claim 1 recites the limitation "supplying the reference voltage to control terminals of a plurality of current-generating active elements". Claims 1 and 13 further recites the limitation "selects some of the plurality of current generating active elements based on signals". It is shown in Fig. 3 that the current-generating active elements with control terminals being supplying by the reference voltage (33a-33f) are clearly selected based on the Vref and not on the signals (34a-34f). These limitations are mutually exclusive and the examiner suggests that the limitations be amended to include a second set of current-generating active elements, which are selected base on signals.

Claim 1 recites the limitation "the signal" on line 6. It is suggested that the limitation be changed to --the signals-- in order to overcome this objection.

Claim 3 recites the limitation "compensating transistor having that reduces" which the examiner suggests be changed to -- compensating transistor that reduces --.

Claim 13 recites the limitation "supplying the reference voltage to control terminals of a plurality of current-generating active elements". Claims 1 and 13 further recites the limitation "supply the reference voltage to control terminals of a plurality of current generating active elements based on the digital luminance gradation data". It is shown in Fig. 3 that the current-generating active elements with control terminals being supplying by the reference voltage (33a-33f) are clearly selected based on the Vref and

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not on the digital luminance gradation data (34a-34f). These limitations are mutually exclusive and the examiner suggests that the limitations be amended to include a second set of current-generating active elements, which are selected base on signals.

Claims 29 and 30 recite the limitation "including a parallel connection of the unit transistor" which the examiner suggest be changed to --has a parallel connection to the unit transistor--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

Claims 8-10, 20-22 and 29-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "almost" in **Claims 8, 9, 20 and 21** is a relative term, which renders the claim indefinite. The term "almost" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Almost is indefinite because the voltages of the different signals can be almost equal depending on the base voltage and the accuracy that is needed.

Claims 8 and 20 recite the limitation "compensating transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. It is suggested that Claims 7 and 19 be changed to depend from Claim 3 and 15 respectively in order to overcome this rejection.

Claims 9 and 21 recite the limitation "compensating transistors" in line 2. There is insufficient antecedent basis for this limitation in the claim. It is suggested that the limitation be changed to -- compensating transistor -- and that Claims 6 and 18 be changed to depend from Claim 3 and 15 respectively in order to overcome this rejection.

Claims 10 and 22 recite the limitation "compensating transistor" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is suggested that Claims 10 and 22 be changed to depend from Claims 3 and 15 respectively in order to overcome this rejection.

Claims 29 and 30 recite the limitation "the unit transistor" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is suggested that Claims 29 and 30 be changed to depend from Claims 7 and 19 respectively in order to overcome this rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-2, 4-7, 13-14, 16-19 and 25-30 rejected under 35 U.S.C. 102(a) as being anticipated by the applicant's admitted prior art.

Regarding independent **Claim 1**, the applicant's admitted prior art teaches an electronic circuit that changes a reference voltage value with a transforming circuit to supply the reference voltage to control terminals of a plurality of current-generating active elements (Fig. 16-17 elements 72 and 75, The reference voltage can either be V_{ref} or 0), establishes a conduction state of the plurality of current-generating active elements, and selects some of the plurality of current generating active elements base on signals and generates a current having a current level corresponding to the signals by superposing currents passing through the current generating active elements selected by the signal, from among the plurality of current-generating active elements (Figs. 16-17, elements 73 77 and 79, Pg. 2 paragraphs [0008-0010]).

Regarding independent **Claim 2**, the applicant's admitted prior art teaches an electronic circuit, comprising:

- a plurality of current-generating active elements (Fig. 17 element 78);

- a transforming circuit that generates an applied voltage that is applied to control terminals of the plurality of current-generating active elements by changing a reference voltage (Figs. 16-17, elements 72 and 75); and

- selection transistors connected in series to each of the plurality of current-generating active elements (Fig. 17, element 77),

- a current having a current level corresponding to signals being generated by superposing the currents that pass through a selection transistor in which an ON-state is selected, among the selection transistor, based on the signal and the current-generating active elements connected in series to the selected selection transistor from

among the plurality of current-generating active elements (Figs. 16-17, elements 73 77 and 79, Pg. 2 paragraphs [0008-0010]).

Regarding independent **Claim 13**, the applicant's admitted prior art teaches an electro-optical device (Pg. 1 paragraph [0001]), comprising:

a control circuit that outputs digital luminance gradation data (Figs. 16 and 17, Pg. 2 paragraph [0008] the gradation data for transistors 77a-f must inherently come from a control circuit);

a driving circuit that generates an analog driving signal base on the digital luminance gradation data (Fig. 17); and

a pixel circuit that drives an electro-optical element based on the analog driving signal (Fig. 16, Pg. 1 paragraph [0006]),

the driving circuit changing a reference voltage value with a converting circuit to supply the reference voltage to control terminals of a plurality of current-generating active elements and to establish a conduction state in the plurality of current-generating active elements, and selecting some of the plurality of current generating active elements base on the digital luminance gradation data, and superposing currents that pass through a current-generating active elements selected by the digital luminance gradation data, from among the plurality of current-generating active elements, thereby generate an analog driving signal having a current level corresponding to the digital luminance gradation data (Figs. 16-17, elements 73 77 and 79, Pg. 2 paragraphs [0008-0010]).

Regarding independent **Claim 14**, the applicant's admitted prior art teaches an electro-optical device (Pg. 1 paragraph [0001]), comprising:

a control circuit that outputs digital luminance gradation data (Figs. 16 and 17, Pg. 2 paragraph [0008] the gradation data for transistors 77a-f must inherently come from a control circuit);

a driving circuit that generates an analog driving signal base on the digital luminance gradation data (Fig. 17); and

a pixel circuit that drives an electro-optical element based on the analog driving signal (Fig. 16, Pg. 1 paragraph [0006]),

the driving circuit comprising a plurality of current-generating active elements; a transforming circuit that generates an applied voltage which is applied to control terminals of the plurality of current-generating active elements by changing a reference voltage; and selection transistors connected in series to each other plurality of current-generating active elements (Fig. 17), and

a current having a current level corresponding to the digital luminance gradation data being generating by superposing the current that pass through a selection transistor in which an ON-state is selected, from among the selection transistor, base on the signal and the current-generating active elements connected in series to the selected selection transistor from among the plurality of current-generating active elements (Figs. 16-17, elements 73 77 and 79, Pg. 2 paragraphs [0008-0010]).

Regarding **Claims 4 and 16**, the admitted prior art further teaches that each of the current-generating active elements includes at least one transistor (Fig. 17).

Regarding **Claims 5 and 17**, the admitted prior art further teaches that the current-generating active elements are connected in parallel to each other (Fig. 17).

Regarding **Claims 6 and 18**, the admitted prior art further teaches that each of the current-generating active elements comprise one current generating transistor and the current generating transistor have different gain factors from each other (Fig. 17, Pg. 2 paragraph [0011]).

Regarding **Claims 7 and 19**, the admitted prior art further teaches at least one current generating active element from among the plurality is connected in series to a unit transistor (Fig. 17, Pg. 2 paragraph [0011] Transistor 78a would be considered the unit transistor and transistor 77a would be connected in series with 78a).

Regarding **Claims 25 and 26**, the admitted prior art further teaches that the electro-optical element is an electroluminescent element comprising a light-emitting layer made of organic materials (Pg. 1 paragraph [0002-0003]).

Regarding **Claims 27 and 28**, the admitted prior art further teaches an electronic apparatus packaged with the electronic circuit (Pg. 1 paragraph [0001-0003]).

Regarding **Claim 29 and 30**, the admitted prior art further teaches at least one current generating active element of the plurality of current generating active elements has a parallel connection to the unit transistor (Fig. 17, Pg. 2 paragraph [0011] Transistor 78a would be considered the unit transistor and the rest of the transistor would therefore be connected in parallel to 78a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 8-12, 15, and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art in view of Kimura (US 6,362,798).

Regarding **Claims 3 and 15**, the applicant's admitted prior art fails to teach a compensating transistor as claimed. Kimura teaches a compensating transistor which reduces or increases an input voltage by a predetermined amount (Kimura, Fig. 1 element 120). More specifically the compensating transistor acts to stabilize an input voltage. It would have been obvious to add the compensating transistor as taught by Kimura to the input Vref of the applicant's admitted prior art in order to stabilize the Vref input signal.

Regarding **Claims 8 and 20**, Kimura further teaches that the compensating capacitors should have close characteristics with driving transistors. When the compensating transistor as taught by Kimura is applied to the applicant's admitted prior art as stated above the driving transistor becomes the unit transistor 78a which means that they should preferably have almost the same characteristics as claimed.

Regarding **Claims 9 and 21**, Kimura further teaches that the compensating transistors are formed next to the driving circuitry as well as having almost the same threshold values (Fig. 1 elements 110 and 120, Col. 10 lines 19-25).

Regarding **Claims 10 and 22**, Kimura further teaches an initializing device that turns on the compensating transistor (Kimura, Fig. 1 element 130). Such a device is critical to the operation of the compensating transistor and is therefore inherent in the combination made above.

Regarding **Claims 11-12 and 23-24**, Kimura further teaches a voltage-stabilizing device comprising a capacitor for further stabilizing the voltage for the transforming circuit (Kimura, Fig. 1 element 160). It would have been obvious to one of ordinary skill in the art to add the capacitor as described by Kimura to the transforming circuit in order to maintain the gate voltage of the compensating transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chiang (US 6,317,066)

Janssen (US 6,384,817)

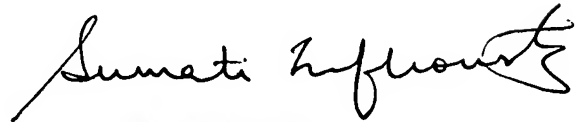
Koyama (US 6,697,057)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 25th, 2005 - kx -

A handwritten signature in black ink, appearing to read "Sumati Lefkowitz", with a stylized flourish at the end.

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER